REMARKS

Claims 1, 2, 10, 11, 19-25, 32 and 33 have been amended. Applicants have amended independent claims 1, 10, 19, 22, and 32 only to clarify the meaning of certain clauses in the claims, and not for patentability reasons. In addition, dependent claims 2, 11, 20, 21, 23-25 and 33 have been amended only to correct informalities, and not for patentability reasons. Claims 1-40 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Section 103(a) Rejections:

The Office Action rejected claims 1-4, 6-13, 15-25, 27-35 and 37-40 under 35 U.S.C. § 103(a) as being unpatentable over Perotto et al. (U.S. Patent 5,630,130) (hereinafter "Perotto"), and claims 5, 14, 26 and 36 as being unpatentable over Perotto in view of Applicant Admitted Prior Art (hereinafter "AAPA"). Applicant respectfully traverses these rejections for at least the following reasons.

Claim 1 of the present application recites, in part, a resource access control mechanism for a multi-thread computing environment operable to manage a **sequence of one or more mutexes associated with a resource**, and, when a requesting thread attempts an access to the resource, to lock a mutex, **to make a determination whether the sequence includes a previous mutex**, and **if a result of the determination is positive, to attempt to lock the previous mutex**.

In rejecting claim 1, the Examiner first asserts that Perotto discloses "one or more mutexes, wherein **the sequence of mutexes is associated with a resource**" and cites col. 5, lines 5 – 6 of Perotto in support of this assertion. In col. 5, lines 3 – 12, Perotto discloses:

> The ALU 11 and the RAM 12 are shared resources and can be accessed by all tasks executed by the controller 1. Semaphores are used to control access to the shared resources of the controller 1 in the following manner. When a task uses a shared resource, a bit in a selected data register is set

> busy. When this task has finished using the shared resource, this bit is set free. The state of this bit is tested by all tasks wishing to access a shared resource, and if the bit has been set busy by earlier task, the later task must wait until the bit is set free.

The Examiner then asserts that Perotto discloses "to attempt to lock a previous mutex in sequence if present", and cites col. 5, lines 8 – 12, and "col. 5, line 66 – col. 5 line 5" in support of this assertion. (Applicant assumes that the Examiner intended to cite col. 5, line 66 – col. **6**, line 5.) The Examiner's interpretation of Perotto is incorrect. Perotto's teachings of col. 5, lines 8 – 12 have been quoted above. Col. 5, line 66 – col. 6, line 5 of Perotto state:

> The scheduler 7 executes, in turn, an instruction of each active task according to a circular priority scheme. Thus, if each of the four tasks are active, the scheduler 7 executes sequentially one instruction of each task. If, however, only one task is active, the scheduler 7 executes sequentially the instructions of that task without any delay, and acting in this way as a monoprocessor.

Applicant can find no teaching or suggestion anywhere in Perotto of when a requesting thread attempts an access to the resource, to lock a mutex, **to make a determination whether the sequence includes a previous mutex**, and **if a result of the determination is positive, to attempt to lock the previous mutex**, as recited in claim 1. As described in the portions of Perotto cited by the Examiner, for any particular access of a shared resource Perotto's system only checks the particular semaphore for that resource.

The Examiner then acknowledges that "Perotto does not explicitly teach that managing a sequence of one or more mutexes." This acknowledgment appears to contradict the Examiner's previous assertions discussed above, where the Examiner cited various lines of Perotto as teaching "a sequence of mutexes associated with a resource", and "attempting to lock a previous mutex in the sequence".

Next, the Examiner asserts that because Perotto teaches "semaphores are use to control access to a shared resource", it would have been obvious to "apply the teaching of Perotto because Perotto's managing a sequence of mutexes as claimed would increase the flexibility of Perotto's system by providing the step of managing mutexes to increase the

effective size of the task performed by the microprocessor and reduce its operating speed and power consumption". The Examiner's reasoning for modifying Perotto's teachings is improper. Nothing about a teaching that "semaphores are used to control access to a shared resource" makes obvious **managing a sequence of one or more mutexes** associated with a resource, and when a requesting thread attempts an access to the resource, **to lock a mutex and to make a determination whether the sequence includes a previous mutex,** and **if a result of the determination is positive, to attempt to lock the previous mutex**, as recited in claim 1. The Examiner is no doubt aware that, in order to establish a *prima facie* obviousness of a claimed invention, **all claim limitations must be taught or suggested by the prior art**. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Obviousness cannot be established by combining or modifying the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion or incentive to do so. *In re Bond,* 910 F. 2d 81, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990). The Examiner's motivation of "to increase the effective size of the task performed by the microprocessor and reduce its operating speed and power consumption" provides no reason whatsoever to modify Perotto's system to function as recited in Applicant's claim 1. Also, Perotto teaches away from the reasoning given by the Examiner. Perotto refers to large task sizes and reduced operating speed as "disadvantages of the prior art" (col. 2, line 32), rather than desirable goals to achieve. *See, e.g.*, col. 1, line 66 – col. 2, line 5 of Perotto: "This manner of execution, though commonly used elsewhere in the computer industry, is nevertheless **not well suited** to the horological domain. The **burden** of the extra instructions introduced by the scheduler **increases the effective size of the tasks** performed by the microprocessor and equally **reduces its performance in terms of speed** and power consumption."

Independent claims 10, 19, 22 and 32 each recite limitations using language similar to that of claim 1, and the rejection of these claims is improper for similar reasons as discussed above.

In regard to claims 6-9, 15-18, 27-30 and 37-40, the Examiner states that it would have been obvious to one of ordinary skill in the art to have included an array, a ring buffer, a link list and a circular linked list [in Perotto's system] because they would be desirable to perform the customization the most efficient manner possible. Applicant does not understand what the Examiner means by "to perform the customization the most efficient manner possible." The reason does not appear to have anything to do with using an array, a ring buffer, a link list and a circular linked list to hold a sequence of mutexes. Furthermore, while such data structures may be well known in the prior art **for other purposes**, the prior art does not teach or suggest the use of an array, a ring buffer, a link list or a circular linked list to hold a sequence of mutexes. Moreover, it would not make sense to use such structures in Perotto's system because Perotto's system only employs a single semaphore per shared resource. The Examiner has not cited any art that teaches or suggests the use of an array, a ring buffer, a link list or a circular linked list to hold a sequence of mutexes. Therefore, the rejection of these claims is improper.

Applicant also asserts that numerous other ones of the dependent claims recited further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicants submit the application is in condition for allowance, and notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above referenced application from becoming abandoned, Applicant hereby petitions for such extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-67700/RCK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

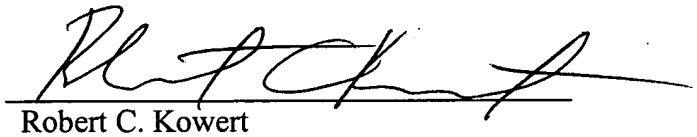
☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Fee Authorization Form authorizing a deposit account debit in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



Robert C. Kowert
Reg. No. 39,255
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C.
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8850

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